UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. MEDIATEK, INC. and MEDIATEK USA, INC., Defendants.	Case No. 7:24-cv-00029-DC-DTG

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES

Page(s)

Cases

I. INTRODUCTION

Defendants' claim construction positions should be adopted because the disputed claim phrases are not described in the specification and are subjective terms of degree for which no adequate, objective boundaries are provided in the intrinsic evidence. These terms therefore fail to inform those skilled in the art about the scope of the claimed invention with reasonable certainty and are indefinite.[1]

II. BACKGROUND

A. Procedural History

Plaintiff filed its Complaint on January 26, 2024, alleging that Defendants' "SoC products comprising two or more sets of processors supporting or based on the DynamIQ Shared Unit architecture (*e.g.*, ARMv8.2, ARMv9 ARMv9.2, and successors), including without limitation the MediaTek Dimensity 9000+ a.k.a. MT6983)" infringe U.S. Patent No. 8,549,339 (the "'339 Patent"). Dkt. No. 1 at ¶ 9; Declaration of Christopher Kao ("Kao Decl."), Ex. A ('339 Patent) at 1. Plaintiff served infringement contentions on August 15, 2024, alleging infringement of Claims 1, 5, 8-10, 14, and 21 of the '339 Patent.

MediaTek filed a petition for *inter partes* review ("IPR") of Claims 1-6, 8-11, 14, and 21 of the '339 Patent (i.e., all claims asserted here and others) on October 22, 2024. *MediaTek Inc. v. Redstone Logics LLC*, IPR2025-00085. Plaintiff's preliminary response is due by December 30, 2024, and the Patent Trial and Appeal Board ("PTAB") must issue an institution decision by March 30, 2025.

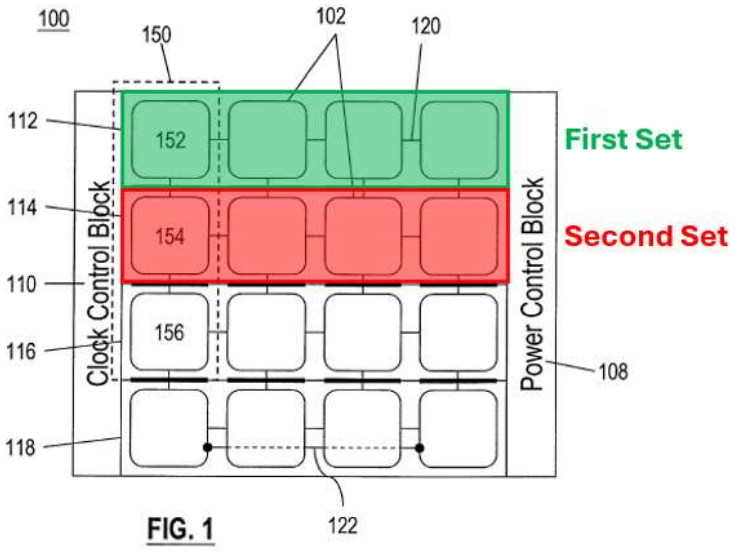
The *Markman* hearing in this action is currently scheduled for February 19, 2025. Dkt. No. 28 at 2. The *Markman* hearing in Plaintiff's other pending case on the '339 Patent is also set for

[1] "MediaTek" refers to Defendants MediaTek Inc. and MediaTek USA, Inc.

February 19, 2025. *Redstone Logics LLC v. NXP Semiconductors N.V. et al*., No. 7:24-cv-00028-DC-DTG, Dkt. No. 36 at 2 (W.D. Tex.). During the meet-and-confer process, the parties were able to agree to the construction of one disputed term (proposed by Plaintiff) to narrow the disputes for resolution.

B. The '339 Patent

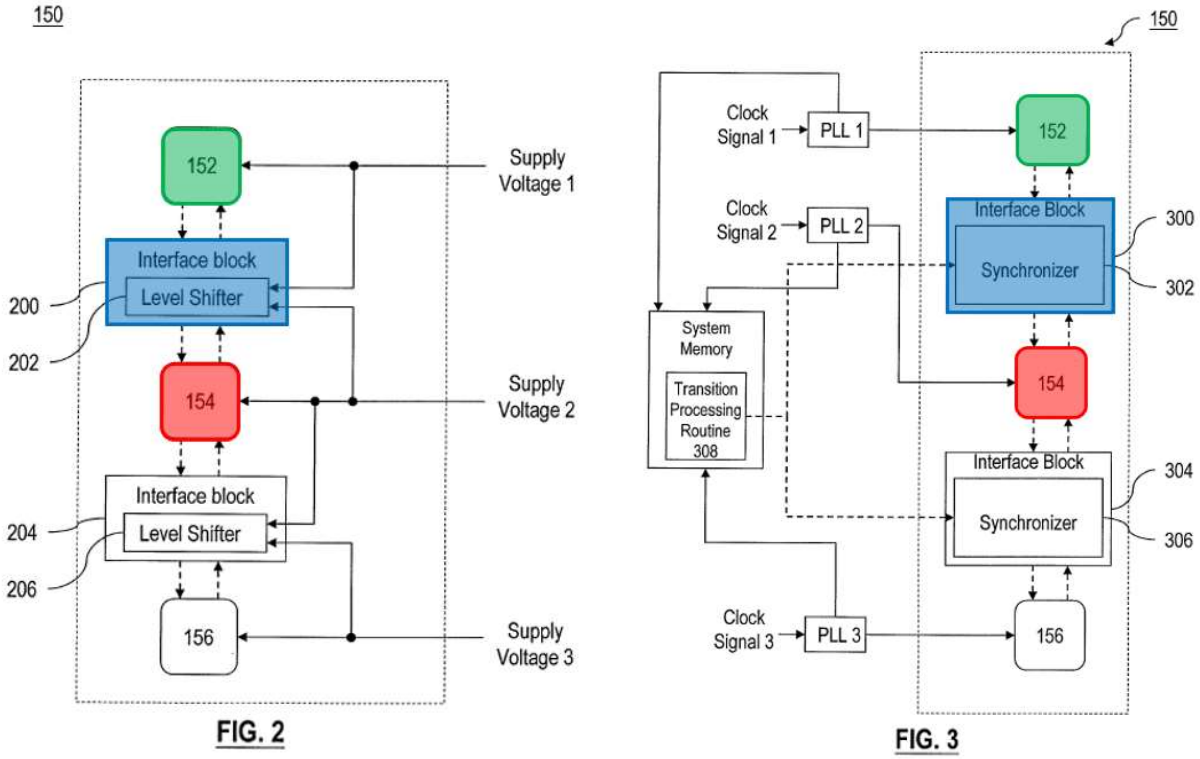
The '339 Patent discloses providing sets of processor cores with independent voltage and clock signals so that the multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced. '339 Patent at Abstract, 1:10-14, 2:25-31. Figure 1 shows four sets of processor cores, with the first set and the second set of processor cores highlighted:



'339 Patent, Fig. 1 (annotated)

Figures 2, below, shows independent voltages supplied to the green set of processor cores and to the red set of processor cores. *Id.* at 2:25-31. And Figure 3, below, shows that independent clock signals ("Clock Signal 1" and "Clock Signal 2") are supplied to separate "phase lock loops" ("PLLs"), one for the green set of cores and one for the red set of cores. *Id.* An "interface block"

is shaded in blue in these figures and is meant to "facilitate communication." *Id.*, 3:21-23, 3:30-34, 4:4-8, Cls. 1, 21.



'339 Patent. Figs. 2 and 3 (annotated)

III. AGREED UPON TERMS

The parties have agreed upon the following construction:[2]

Term	Agreed Construction
"set of processor cores" (Claims 1, 5, 8, 14, 21)	"group of two or more processor cores"

[2] Plaintiff proposed this term for construction and proposed that it mean "set of two or more processor cores," which is circular. Furthermore, MediaTek proposed that this term be afforded its plain and ordinary meaning, but agreed to the construction herein solely as a compromise to streamline the litigation, especially as MediaTek understands that it was agreed to in related litigation, *Redstone Logics LLC v. NXP Semiconductors N.V. et al.*, No. 7:24-cv-00028-DC-DTG (W.D. Tex.). MediaTek's compromise on this term is without prejudice to its right to argue otherwise in another proceeding, such as on appeal or in IPR.

IV. DISPUTED TERMS

A. "each processor core from the first/second set of processor cores is *configured to dynamically receive* a first/second supply voltage [from a power control block] and a first/second output clock signal" (Claims 1, 21)

MediaTek's Proposed Construction	Plaintiff's Proposed Construction
Indefinite	Needs no construction; plain and ordinary meaning

Asserted independent Claims 1 and 21 recite that "each processor core from the first/second set of processor cores is ***configured to dynamically receive*** a first/second supply voltage [from a power control block] and a first/second output clock signal." '339 Patent, Cls. 1 and 21 (emphasis added) (the bracketed language appearing in Claim 21). However, the phrase "configured to dynamically receive," when read in light of the specification, "*fails to inform, with reasonable certainty*, those skilled in the art about the scope of the invention," and therefore renders these claims invalid for indefiniteness. *See Biosig Instruments, Inc. v. Nautilus, Inc*., 783 F.3d 1374, 1378 (Fed. Cir. 2015) (emphasis in original) (quoting *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014)).

"[I]ndefiniteness is a question of law." *IPXL Holdings, L.L.C. v. Amazon.com, Inc*., 430 F.3d 1377, 1380 (Fed. Cir. 2005). When a patent claim includes a term with an unknown meaning or a "term of degree," the patent must provide a "standard for measuring the scope" of the term, and the claims "must provide objective boundaries for those of skill in the art." *Interval Licensing LLC v. AOL, Inc*., 766 F.3d 1364, 1370-71 (Fed. Cir. 2014). Claims having terms of degree are indefinite when the patent fails to provide objective guidance for determining their scope. *See, e.g., id*. at 1371-73 (holding subjective term "unobtrusive manner" indefinite, using similar analysis to that for terms of degree); *Dow Chem. Co. v. Nova Chems. Corp. (Can.)*, 803 F.3d 620,

633-35 (Fed. Cir. 2015) (holding term of degree indefinite for lacking guidance as to how it should be measured).

Here, the phrase "configured to dynamically receive" is not a term of art, has an unknown meaning in this context, and could be a subjective term of degree. Declaration of R. Jacob Baker, Ph.D. ("Baker Decl.," filed herewith), ¶¶37-43. The claims and specification do not explain or provide any guidance on how to distinguish processor cores that are configured to dynamically receive a supply voltage or clock signal from cores that are configured to receive such signals statically or not dynamically. *Id*., ¶37. Indeed, the phrase "configured to dynamically receive" only appears in Claims 1 and 21 and nowhere else in the specification. Likewise, the prosecution history of the '339 Patent provides no guidance as to the claim scope of what it means for a processor core to be "configured to dynamically receive" supply voltages and clock signals. Kao Decl., Ex. B.

To a person of ordinary skill in this art (a "PHOSITA"), "configured to dynamically receive," does not have an understood meaning, and the lack of any context in the '339 Patent exacerbates this problem. *Id*., ¶38. While the phrase "configured to dynamically receive" does not appear anywhere in the specification of the '339 Patent except Claims 1 and 21, the patent does disclose processor cores that are simply "configured to receive" signals, which is a common function of processor cores. *Id*., ¶39. For example, Claims 5 and 14 recite, "wherein the first set of processor cores and the second set of processor cores ***are configured to receive*** one or more control signals from one or more control blocks." *Id*. A PHOSITA would not have reasonable clarity here, though, because the '339 Patent does not explain how a processor core "configured to ***dynamically*** receive" voltage and clock signals, as recited in Claims 1 and 21, is different from receiving voltage and clock signals non-dynamically. *Id*.

"While a PHOSITA would understand that the term 'dynamic' conveys something that is changing as opposed to something that remains the same or 'static,' a PHOSITA would not know whether 'dynamically' refers to changes (e.g., in time, voltage levels, frequencies, etc.) above a specific threshold or even what that threshold might be." *Id.*, ¶40. Similarly, a PHOSITA could understand that voltage and clock frequencies can be adjusted in response to processing requirements or power consumption needs, "a PHOSITA would not know whether the modifier, 'dynamically,' connotes a specific threshold rate at which those changes occur and/or a specific threshold regarding the degree of those changes." *Id.* In sum, "a PHOSITA is left in the dark after reading the intrinsic evidence regarding what the metes and bounds of [configured to dynamically receive] is and what objective standards could be used to determine whether a particular processor cores was 'dynamically' receiving signals, given the varying changes and fluctuations that could be involved." *Id.*, ¶41.

Because the claims, specification, and prosecution history provide no reasonable clarity on the scope of the claim term, "configured to dynamically receive," Claims 1 and 21 thus contain a subjective "term of degree" or an unknown term whose interpretation "depends 'on the unpredictable vagaries of any one person's opinion.'" *See Interval Licensing*, 766 F.3d at 1371 (citing *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1350 (Fed. Cir. 2005)). The claims are therefore indefinite because there is no objective standard provided for what determines how a processor core can be "configured to dynamically receive" voltage supply and clock signals. *See, e.g., Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1255 (Fed. Cir. 2008); *CardWare Inc. v. Samsung Elecs. Co.*, No. 2:22-CV-141-JRG-RSP, 2023 WL 5434763, at *26 (E.D. Tex. Aug. 23, 2023) (finding "dynamically generating" indefinite for failing to "inform those skilled in the art about the scope of the invention with reasonable certainty" because, among other

reasons, "the intrinsic record does not provide insight" regarding that term) (citing *Nautilus*, 572 U.S. at 910).

B. "one or more control blocks located in a periphery of the multi-core processor" (Claim 5)

MediaTek's Proposed Construction	Plaintiff's Proposed Construction
Indefinite	Needs no construction; plain and ordinary meaning

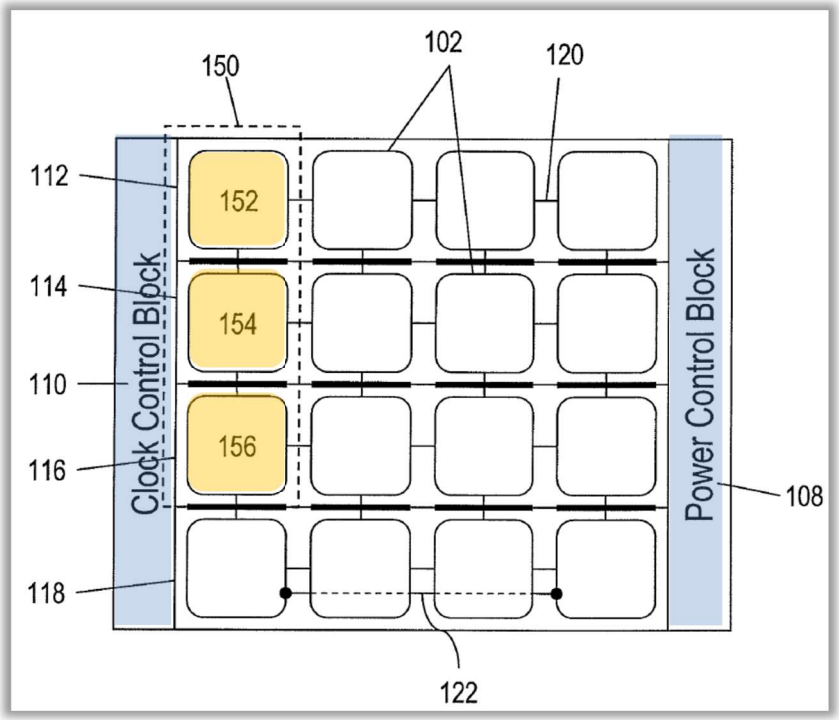
Claim 5 of the '339 Patent recites that the first set of processor cores and second set of processor cores of the "multi-core processor of claim 1" are "configured to receive one or more control signals from one or more control blocks located in a ***periphery*** of the multi-core processor." '339 Patent, Cl. 5 (emphasis added). However, the undefined term of degree, "periphery," only appears in one place in the specification: "A power profile associated with an individual processor core may be controlled through signals that may be received from control blocks that are located in the periphery of the multi-core processor." '339 Patent at 1:61-65. Thus, in the only place where this term is discussed, no guidance is provided on how to measure the bounds of what constitutes the "periphery" of the processor with any degree of certainty for a PHOSITA. Baker Decl., ¶44; *see generally id*., ¶¶44-52.

This problem is compounded by the apparent contrasting of locations in other parts of the specification. In particular, the '339 Patent discloses that "the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100" or "at the same side," which is contrasted with other implementations where "the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100":

> The multi-core processor 100 may be further divided into regions. In some implementations, the regions of multi-core processor 100 may correspond to rows of the two-dimensional array, and the regions may or may not be overlapping. Each

> row of processors may also be referred to as a "stripe." For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. Each stripe may be associated with an independent power profile. For example, the stripe 112 may be powered by a supply voltage received from a power control block 108 and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block 110. In some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100 as shown in FIG. 1. In some other implementations, the power control block 108 and the clock control block 110 may be arranged at the same side of the multi-core processor 100. In yet some other implementations, the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100.

'339 Patent at 2:20-40. "As seen above, this part of the specification does not discuss where the periphery is located or the bounds of that apparent region of the processor, but it states that an arrangement of control blocks on 'two different sides of the multicore processor' are 'shown in FIG. 1.'" Baker Decl., ¶46. Figure 1 (below, with **blue** highlighting around the control blocks and **orange** highlighting around the processor cores), shows those blocks at the very edge of the processor core:



However, there is no indication that this necessarily corresponds to the "periphery" of the processor, or how to draw the box of what constitutes the "edge" or "periphery. Baker Decl., ¶47. This confusion is amplified by other figures in the '339 Patent. For instance, Figure 3 shows the same cores 152, 154, and 156 from Figure 1. But, again, there is no indication of where the control blocks would be, whether at the periphery or centrally located or some other configuration. *Id*. And if the control blocks are placed right next to the processor cores, as in Figure 1, then the imaginary line around the periphery becomes even more blurred. This is represented in Figure 3 below, in which it is unclear where the periphery is located for housing the control blocks, as it could be any undefined space around the processor cores (an undefined region highlighted in **blue** for possible control block locations is shown below, in which the undefined region could extend into what could be considered both central and peripheral locations according to conflicting disclosures in the '339 Patent). This shows that the location is an arbitrary and subjective determination without objective guidance in the '339 Patent.

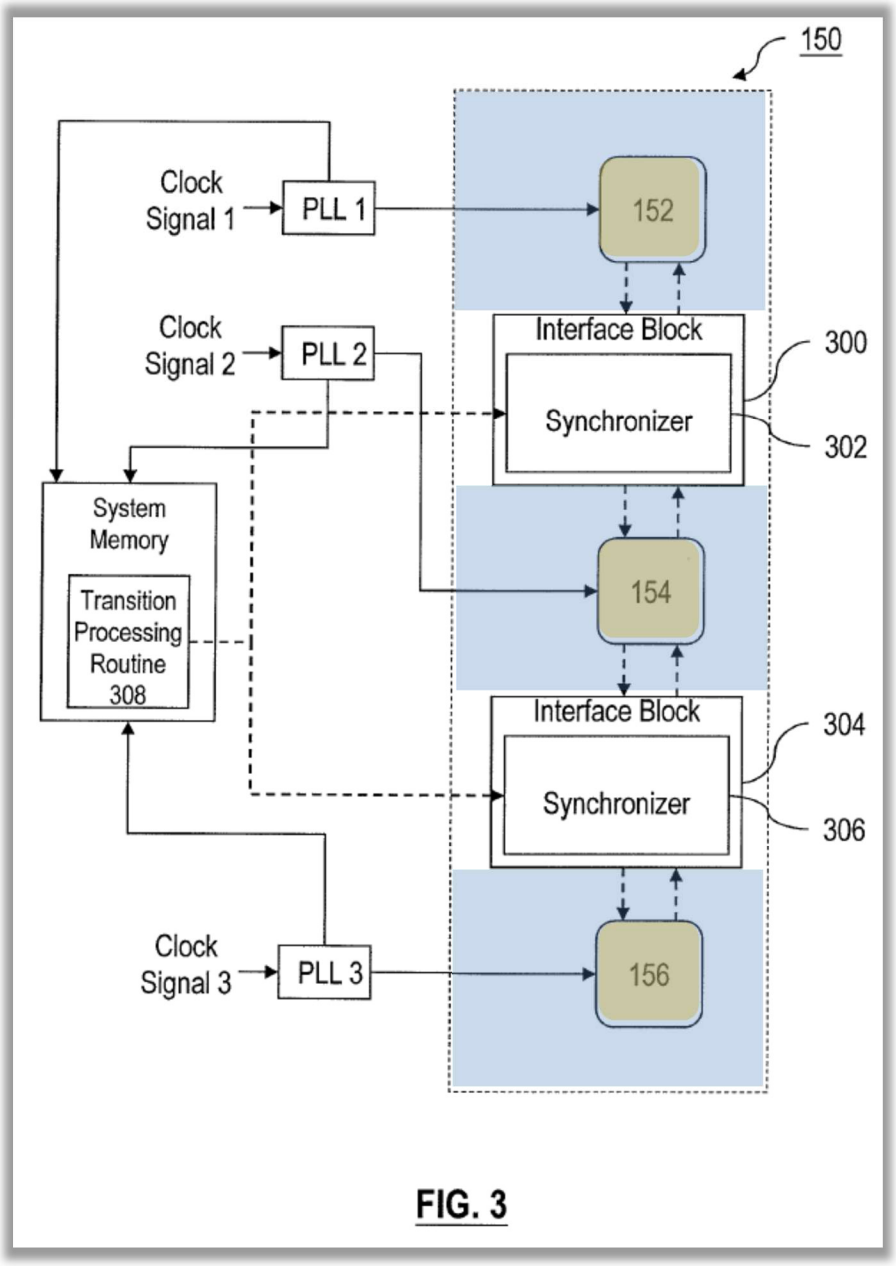


FIG. 3

See also Baker Decl., ¶47.

The lack of clarity in the intrinsic evidence is additionally problematic because there is not a common understanding in this field regarding what constitutes the "periphery" of a "multi-core processor." *Id.*, ¶50. While a POSITA understands what a "multi-core processor" is, a "PHOSITA would also know that it might refer to multiple components or arrangements." *Id.*, ¶49. For example, a PHOSITA could refer to multiple individual processor cores (e.g., processor cores 152,

154, and 156 in Figure 1, above) as a multi-core processor. *Id*. In other situations, a PHOSITA may consider the complete die, containing the processor cores and additional circuitry, to be a "multi-core processor." *Id*. A PHOSITA could also refer to the packaged die as a "multi-core processor." *Id*. "As such, it is unclear whether 'periphery of the multi-core processor' might be limited to regions inside the multi-core processor within some unspecified distance of the boundary of the multi-core processor, however that boundary might be defined, or whether 'periphery of the multi-core processor' also includes components outside the multi-core processor but within some unspecified distance of its boundary." *Id*.

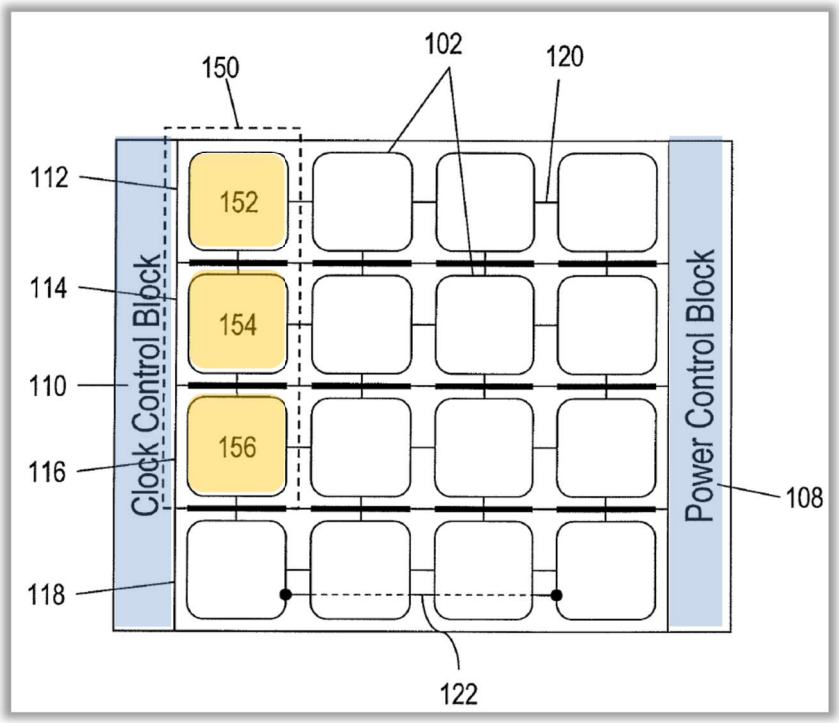
Because the claims, specification, and prosecution history provide no reasonable clarity on the scope of the claim term, "located in a periphery of the multi-core processor," Claim 5 thus contains a subjective "term of degree" or an unknown term whose interpretation "depends 'on the unpredictable vagaries of any one person's opinion.'" *See Interval Licensing*, 766 F.3d at 1371. The claim is therefore indefinite because there is no objective standard provided for the bounds of the "periphery" of the claimed multi-core processor in the context of the '339 Patent. *See, e.g., Halliburton Energy Servs.*, 514 F.3d at 1255; *Int'l Test Sols., Inc. v. Mipox Int'l Corp*., No. 16-CV-00791-RS, 2017 WL 1367975, at *5 (N.D. Cal. Apr. 10, 2017) (ruling "predetermined characteristics" indefinite because "[n]owhere is a complete embodiment of the [device's] 'predetermined characteristics' described;" and "[n]or does the patent offer any guidance on the relationship between the different characteristics"); *Skyhook Wireless, Inc. v. Google, Inc*., No. CIV.A. 10-11571-RWZ, 2014 WL 898595, at *4 (D. Mass. Mar. 6, 2014) (ruling that the term "estimated characteristics" is indefinite because the claims and specification do not "provide any insight into the proper construction").

C. "common region that is substantially central to the first set of processor cores and the second set of processor cores" (Claim 14)

MediaTek's Proposed Construction	Plaintiff's Proposed Construction
Indefinite	Needs no construction; plain and ordinary meaning

This phrase suffers from some of the same ambiguity as the "periphery" term, above. This disputed phrase is part of the larger limitation of Claim 14 of the '339 Patent, which recites "wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks ***located in a common region that is substantially central*** to the first set of processor cores and the second set of processor cores." '339 Patent, Cl. 4 (emphasis added). The intrinsic evidence does not inform a PHOSITA of the scope of this phrase with reasonable certainty. *See also* Baker Decl., ¶¶53-64.

Again, this problem is compounded by the apparent contrasting of locations in the specification of the '339 Patent. The '339 Patent discloses that "the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100" or "at the same side," which is contrasted with other implementations where "the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100." '339 Patent at 2:20-40. This part of the specification does not discuss where the disclosed regions are of the processor or their bounds. Baker Decl., ¶56. Again, an arrangement of control blocks on "two different sides of the multicore processor" are "shown in FIG. 1." Figure 1 (below, with **blue** highlighting around the control blocks and **orange** highlighting around the processor cores), shows those blocks at the very edge of the processor core:



There is no indication that this shows a "common area" or one that is "substantially central" to two sets of processor cores. This confusion is amplified by other figures in the '339 Patent. For instance, Figure 3 shows the same cores 152, 154, and 156 from Figure 1. But, again, there is no indication of where the control blocks would be, whether at the periphery or centrally located or some other configuration. Baker Decl., ¶57. This is represented in Figure 3 below, in which it is unclear where the "common area" is located or whether that area is "substantially central" to the cores, or what that box is defined to be (an undefined region highlighted in **blue** for possible control block locations is shown below, in which the undefined region could extend into what could be considered both central and peripheral locations according to conflicting disclosures in the '339 Patent). This shows that the location is an arbitrary and subjective determination without objective guidance in the '339 Patent.

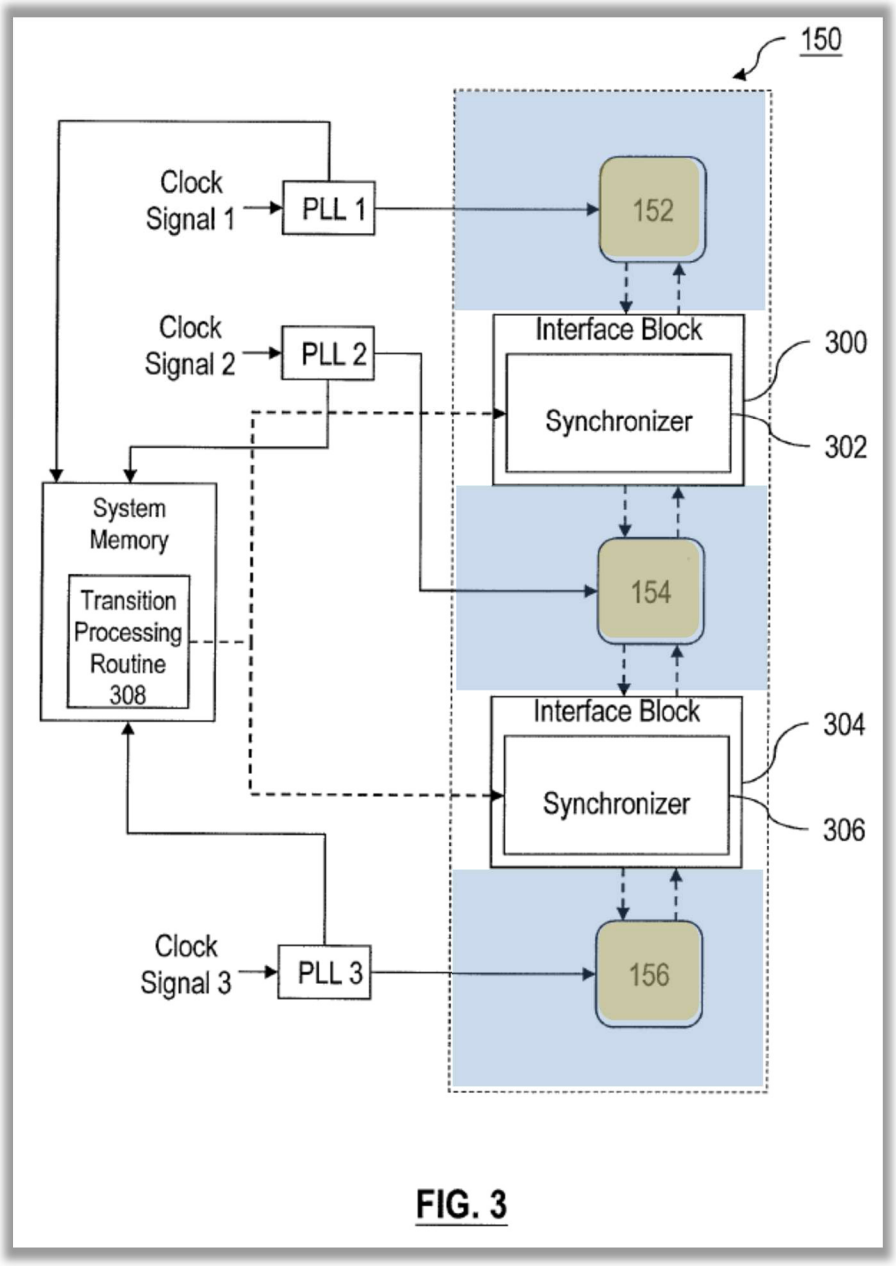


FIG. 3

See also Baker Decl., ¶57.

Furthermore, as with the subjective "periphery" term above, neither "located in a common region" nor "substantially central" have a common understanding in this field such that a POSITA could determine with reasonably certainty what constitutes components "located in a common region" or whether such components are "substantially central" to the first and second sets of processor cores. Baker Decl., ¶59. The '339 Patent does not provide the necessary context or

bounds for this vague term. The claim language does not shed any light regarding what constitutes a common region. While Claim 14 references a "common region," other claim language creates ambiguity regarding what that means. Claim 8, for instance, which like Claim 14 depends directly from Claim 1, recites that the processor cores as located in a "region." Specifically, Claim 8 states "the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor." A PHOSITA would not understand with reasonable certainty what delineates a region or what it means for such a "region" to be "common" between the first and second sets of processor cores. Baker Decl., ¶60. One reasonable interpretation of "common" would be "overlapping." But "overlapping" regions are explicitly recited in Claim 9, which depends from Claim 8 and states, in part, "wherein the first region and the second region are overlapping regions." Thus, the '339 Patent further causes confusion for a PHOSITA because while "common" could be interpreted to mean "overlapping," the '339 Patent actually distinguishes "common" and "overlapping." This confirms that a PHOSITA would not reasonably understand the metes and bounds of a "common region" in the context of the '339 Patent. Baker Decl., ¶60.

Furthermore, the claims and the specification do not inform a PHOSITA as to the scope of the phrase "substantially central," nor what it means for a "common region" to be "substantially central" to the first and second sets of processor cores. *Id.*, ¶61. Indeed, the phrase "substantially central" is never used in the specification.

As discussed above for the "peripherally located" phrase, there are many different arrangements for multi-core processors. Without further guidance from the '339 Patent, and there is none, a PHOSITA would not understand where "substantially central" is to be measured from and how to do so. *Id.*, ¶62. For instance, in an arrangement where processor cores are in rows at

various points on the die, such as at the top corners, it would be unclear whether "substantially central" would be in reference to the center of the die (i.e., in the center when measured from the vertical center line) or a reference to some middle point on the same horizontal center line as the two rows of processor cores. *Id*. "In other words, 'substantially central' is a term of degree for a PHOSITA, and the '339 Patent does not provide any objective criteria from which to measure that degree. *Id*.

Claim 14 is therefore indefinite because there is no objective standard provided for the bounds what is the "common region that is substantially central to the first set of processor cores and the second set of processor cores" of the claimed multi-core processor in the context of the '339 Patent. *See, e.g., Interval Licensing*, 766 F.3d at 1371; *Halliburton Energy Servs.*, 514 F.3d at 1255; *Int'l Test Sols.*, 2017 WL 1367975, at *5; *Skyhook Wireless*, 2014 WL 898595, at *4.

V. CONCLUSION

For the foregoing reasons, MediaTek respectfully requests that the Court adopt its claim construction positions and find the disputed phrases of the '339 Patent indefinite.

Dated: December 4, 2024

Respectfully submitted,

By: */s/ Christopher Kao*

Christopher Kao (*admitted*)
christopher.kao@pillsburylaw.com
Brock S. Weber (*admitted*)
brock.weber@pillsburylaw.com
Pillsbury Winthrop Shaw Pittman LLP
4 Embarcadero Center, 22nd Floor
San Francisco, CA 94111
Telephone: 415.983.1000
Facsimile: 415.983.1200

Counsel for Defendants
MediaTek USA Inc. and MediaTek Inc.

CERTIFICATE OF SERVICE

I certify that on December 4, 2024, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Christopher Kao
Christopher Kao